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				Filing Date	07-22-03	
				First Named Inventor	Jong-Jan Lee	
				Group Art Unit	1763	
LIST OF PRIOR ART CITED BY APPLICANT (use as many sheets as necessary)				Examiner Name	Goudreau	
				Attorney Docket No.	SLA.0696	
Sheet	1	of	1			

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	U.S. Patent Document Kind Number	Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YY	Pages, Columns, Lines, Where Relevant Passages or Figures Appear

FOREIGN PATENT DOCUMENTS								
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, country where published, source.	T ²
gag		M. JURCZAK ET AL., SON (Silicon on Nothing) - A New Device Architecture for the ULSI Era, VLSI Tech. Dig., p.29, (1999).	✓
		R. KOH, Buried Layer Engineering to Reduce the Drain-Induced Barrier Lowering of Sub-0.05um SOI-MOSFET Jpn. J. Appl. Phys., Vol. 38, P. 2294 (1999)	✓
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Examiner Signature	George Goudreau	Date Considered	4-05'
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